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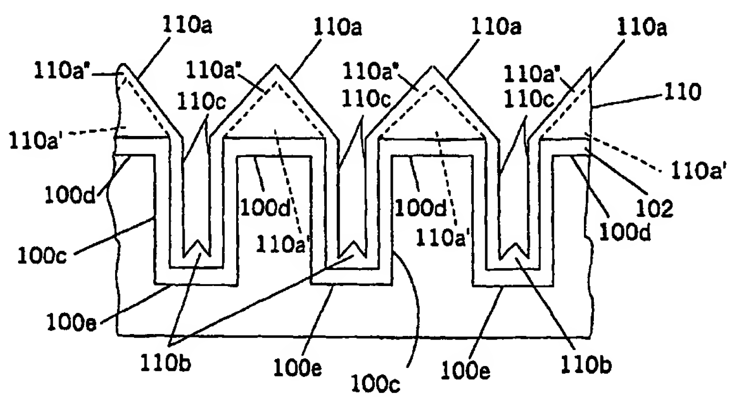
(54) Title: METHODS OF FABRICATING GALLIUM NITRIDE SEMICONDUCTOR LAYERS ON SUBSTRATES INCLUDING NON-GALLIUM NITRIDE POSTS, AND GALLIUM NITRIDE SEMICONDUCTOR STRUCTURES FABRICATED THEREBY



(57) Abstract: A substrate includes non-gallium nitride posts that define trenches therebetween, wherein the non-gallium nitride posts include non-gallium nitride sidewalls and non-gallium nitride tops and the trenches include non-gallium floors. Gallium nitride is grown on the non-gallium nitride posts, including on the non-gallium nitride tops. Preferably, gallium nitride pyramids are grown on the non-gallium nitride tops and gallium nitride then is grown on the gallium nitride pyramids. The gallium nitride pyramids preferably are grown at a first temperature and the gallium nitride preferably is grown on the pyramids at a second temperature that is higher than the first temperature. The first temperature preferably is about 1000 °C or less and the second temperature preferably is about 1100°C or more. However, other than temperature, the same processing conditions preferably are used for both growth steps. The grown gallium nitride on the pyramids preferably coalesces to form a continuous gallium nitride layer. Accordingly, gallium nitride may be grown without the need to form masks during the gallium nitride growth process. Moreover, the gallium nitride growth may be performed using the same processing conditions other than temperatures changes. Accordingly, uninterrupted gallium nitride growth may be performed.

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METHODS OF FABRICATING GALLIUM NITRIDE SEMICONDUCTOR LAYERS ON SUBSTRATES INCLUDING NON-GALLIUM NITRIDE POSTS, AND GALLIUM NITRIDE SEMICONDUCTOR STRUCTURES FABRICATED THEREBY

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Field of the Invention

This invention relates to microelectronic devices and fabrication methods, and more particularly to gallium nitride semiconductor devices and fabrication methods therefor.

Background of the Invention

Gallium nitride is being widely investigated for microelectronic devices including but not limited to transistors, field emitters and optoelectronic devices. It will be understood that, as used herein, gallium nitride also includes alloys of gallium nitride such as aluminum gallium nitride, indium gallium nitride and aluminum indium gallium nitride.

A major problem in fabricating gallium nitride-based microelectronic devices is the fabrication of gallium nitride semiconductor layers having low defect densities. It is known that one contributor to defect density is the substrate on which the gallium nitride layer is grown. Accordingly, although gallium nitride layers have been grown on sapphire substrates, it is known to reduce defect density by growing gallium nitride layers on aluminum nitride buffer layers which are themselves formed on silicon carbide substrates. Notwithstanding these advances, continued reduction in defect density is desirable.

It also is known to produce low defect density gallium nitride layers by forming a mask on a layer of gallium nitride, the mask including at least one opening therein that exposes the underlying layer of gallium nitride, and laterally growing the underlying layer of gallium nitride through the at least one opening and onto the mask. This technique often is referred to as "Epitaxial Lateral Overgrowth" (ELO). The layer of gallium nitride may be laterally grown until the gallium nitride coalesces on the mask to form a single layer on the mask. In order to form a continuous layer of gallium nitride with relatively low defect density, a second mask may be formed on the laterally overgrown gallium nitride layer, that includes at least one opening that is offset from the opening in the underlying mask. ELO then again is performed through the openings in the second mask to thereby overgrow a second low defect density continuous gallium nitride layer. Microelectronic devices then may be formed in this second overgrown layer. ELO of gallium nitride is described, for example, in the publications entitled *Lateral Epitaxy of Low Defect Density GaN Layers Via Organometallic Vapor Phase Epitaxy* to Nam et al., Appl. Phys. Lett. Vol. 71, No. 18, November 3, 1997, pp. 2638-2640; and *Dislocation Density Reduction Via Lateral Epitaxy in Selectively Grown GaN Structures* to Zheleva et al, Appl. Phys. Lett., Vol. 71, No. 17, October 27, 1997, pp. 2472-2474, the disclosures of which are hereby incorporated herein by reference.

It also is known to produce a layer of gallium nitride with low defect density by forming at least one trench or post in an underlying layer of gallium nitride to define at least one sidewall therein. A layer of gallium nitride is then laterally grown from the at least one sidewall. Lateral growth preferably takes place until the laterally grown layers coalesce within the trenches. Lateral growth also preferably continues until the gallium nitride layer that is grown from the sidewalls laterally overgrows onto the tops of the posts. In order to facilitate lateral growth and produce nucleation of gallium nitride and growth in the vertical direction, the top of the posts and/or the trench floors may be masked. Lateral growth from the sidewalls of trenches and/or posts also is referred to as "pendeoepitaxy" and is described, for example, in publications entitled *Pendeo-Epitaxy: A New Approach for Lateral Growth of Gallium Nitride Films* by Zheleva et al., Journal of Electronic Materials, Vol. 28, No. 4, February 1999, pp. L5-L8; and *Pendeoepitaxy of Gallium Nitride Thin Films* by Linthicum et al., Applied Physics Letters, Vol. 75, No. 2, July 1999, pp. 196-198, the disclosures of which are hereby incorporated herein by reference.

Unfortunately, both ELO and pendeoepitaxy may use one or more masks to mask portions of an underlying gallium nitride layer during ELO and/or pendeoepitaxy. These masks may complicate the fabrication process. Moreover, multiple growth steps of gallium nitride may be needed with mask formation therebetween. These multiple growth steps also may complicate the fabrication processes, because the structures may need to be removed from the gallium nitride growth chamber in order to form the mask or masks. Accordingly, notwithstanding the recent advances in ELO and pendeoepitaxy, there continues to be a need for methods of fabricating gallium nitride semiconductor layers that do not need masking layers and/or need not interrupt the gallium nitride growth process.

Summary of the Invention

The present invention provides a substrate including non-gallium nitride posts that define trenches therebetween, wherein the non-gallium nitride posts include non-gallium nitride sidewalls and non-gallium nitride tops, and the trenches include non-gallium floors. These substrates also may be referred to herein as "textured" substrates. Then, gallium nitride is grown on the non-gallium nitride posts, including on the non-gallium nitride tops. Preferably, gallium nitride pyramids are grown on the non-gallium nitride tops and gallium nitride then is grown on the gallium nitride pyramids. The gallium nitride pyramids preferably are grown at a first temperature and the gallium nitride preferably is grown on the pyramids at a second temperature that is higher than the first temperature. The first temperature preferably is about 1000°C or less and the second temperature preferably is about 1100°C or more. However, other than temperature, the same processing conditions preferably are used for both growth steps. The grown gallium nitride on the pyramids preferably coalesces to form a continuous gallium nitride layer.

Accordingly, gallium nitride may be grown on a textured substrate, without the need to provide masks during the gallium nitride growth process. Moreover, the gallium nitride growth may be performed using the same processing conditions other than temperatures changes. Accordingly, uninterrupted gallium nitride growth may be performed. Simplified processing conditions therefore may be employed to grow a gallium nitride layer having low defect densities, for example defect densities of less than about 10^5 cm^{-2}.

During growth of the gallium nitride pyramids on the non-gallium nitride tops, gallium nitride pyramids also may be simultaneously grown on the non-gallium nitride floors. Moreover, a conformal gallium nitride layer also may be formed simultaneously on the sidewalls, between the gallium nitride pyramids on the non-gallium nitride tops and on the non-gallium nitride floors. Upon growing the gallium nitride on the pyramids, the trenches also may be simultaneously filled with gallium nitride. A conformal buffer layer may be formed on the substrate including on the non-gallium nitride sidewalls, the non-gallium nitride tops and the non-gallium nitride floors, prior to growing the gallium nitride pyramids. For example, a conformal layer of aluminum nitride may be used.

Gallium nitride semiconductor structures therefore may be fabricated, according to the present invention, by providing a textured substrate, including a plurality of non-gallium nitride posts that define trenches therebetween, wherein the non-gallium nitride posts include non-gallium-nitride sidewalls and non-gallium nitride tops, and the trenches include non-gallium nitride floors. The substrate preferably is free of masking materials on the non-gallium nitride floors and on the non-gallium nitride tops. Gallium nitride then is grown at a first temperature and the growth of gallium nitride then is continued at a second temperature that is higher than the first temperature. Growth at the second temperature preferably continues until the gallium nitride forms a continuous gallium nitride layer on the substrate.

Gallium nitride semiconductor structures according to the present invention preferably comprise a textured substrate including a plurality of non-gallium nitride posts that define trenches therebetween, the non-gallium nitride posts including non-gallium nitride sidewalls and non-gallium nitride tops, and the trenches including non-gallium nitride floors. A gallium nitride layer is provided on the non-gallium nitride posts including on the non-gallium nitride tops. The gallium nitride semiconductor structure preferably is free of a masking layer on the non-gallium nitride tops and on the non-gallium nitride floors. The gallium nitride layer preferably comprises gallium nitride pyramids on the non-gallium nitride tops. The gallium nitride layer may also include gallium nitride regions on the gallium nitride pyramids. Second gallium nitride pyramids on the non-gallium nitride floors also may be provided. A conformal gallium nitride layer on the sidewalls, between the gallium nitride pyramids and the second gallium nitride pyramids also may be provided. The gallium nitride regions preferably form a continuous gallium nitride layer and the gallium nitride layer also

preferably fills the trenches. A conformal buffer layer also may be provided on the substrate wherein the gallium nitride layer is on the conformal buffer layer opposite the substrate.

The present invention most preferably may be used to provide methods of fabricating gallium nitride semiconductor structures that need not include masking or interruptions during gallium nitride epitaxial growth. Accordingly, simplified processes for fabricating gallium nitride semiconductor structures may be provided, to thereby fulfill a need in the fledgling gallium nitride semiconductor industry. However, it also will be understood that the present invention may be used to fabricate non-gallium nitride semiconductor structures wherein a textured substrate of a first material is provided and a second semiconductor material is grown on the posts including on the tops that comprise the first material. Also, semiconductor structures may be provided including a textured substrate that comprises a first material and a layer of second semiconductor material on the posts that comprise the first material.

Brief Description of the Drawings

Figures 1-6 are cross-sectional views of gallium nitride semiconductor structures during intermediate fabrication steps, according to the present invention.

Detailed Description of Preferred Embodiments

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numbers refer to like elements throughout. It will be understood that when an element such as a layer, region or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. Moreover, each embodiment described and illustrated herein includes its complementary conductivity type embodiment as well.

Referring now to Figures 1-6, methods of fabricating gallium nitride semiconductor structures according to embodiments of the present invention now will

be described. As shown in Figure 1, a substrate **100**, also referred to as a "textured substrate", is provided including a plurality of non-gallium nitride posts **100a** that define trenches **100b** therebetween. The non-gallium nitride posts **100a** include non-gallium nitride sidewalls **100c** and non-gallium nitride tops **100d**. The trenches **100b** also include non-gallium nitride floors **100e**.

It will be understood by those having skill in the art that the substrate **100** may be a monocrystalline substrate or a substrate including one or more monocrystalline layers thereon, from which the posts **100a** and trenches **100b** are defined. Examples of monocrystalline substrates and monocrystalline layers include, but are not limited to, monocrystalline silicon, silicon carbide and/or sapphire. It also will be understood that the posts **100a** and trenches **100b** may be defined using selective etching and/or selective epitaxial growth. Etching may be performed using standard dry or wet etching techniques, preferably using a mask, which then preferably is removed. The fabrication of a substrate including trenches and posts is well known to those having skill in the art and need not be described in detail herein.

As will be shown below, by texturing the substrate **100**, the substrate surface area that is available to contribute to defect formation during subsequent gallium nitride seed deposition may be reduced and preferably minimized. Texturing also may reduce crack formation in the final gallium nitride semiconductor layer by providing stress relief during cooling. Stress may occur due to mismatches in the coefficients of thermal expansion between the substrate material and gallium nitride that is formed subsequently.

It also will be understood that the trenches **100b** preferably are sufficiently deep so that undesirable growth of poor quality gallium nitride from the trench floor **100e** will not interfere with growth of high quality gallium nitride, as will be described below. Moreover, the posts **100a** preferably are grown in the form of stripes that preferably are sufficiently narrow, for example less than or equal to one micron in width, so that small gallium nitride seed pyramids can be formed on the non-gallium nitride tops **100d**. As will be described below, the initial gallium nitride seed pyramids that form on the non-gallium nitride tops **100d** may have defects, so that the reduced size gallium nitride seed pyramids can reduce the total amount of initial defective gallium nitride seed material. The total mechanical stress on the pyramids due to the differences in coefficients of thermal expansion between the substrate, any conformal buffer layers and the grown gallium nitride also may be

reduced, as well as the time to complete the pyramidal growth and initiate pendeoepitaxial growth as will be described below.

When the posts **100a** are in the form of stripes, the stripes preferably extend along the $1\bar{1}00$ direction of a sapphire or silicon carbide substrate **100** and along the **110** direction of a silicon substrate **100**, to thereby expose the $11\bar{2}0$ plane of the subsequently grown gallium nitride layer. In general, the stripes should expose the $11\bar{2}0$ plane of sapphire and silicon carbide substrates. For example, if A-plane sapphire is used, as opposed to C-plane sapphire which is more common, then the wafer flat is the 0001 direction. In order to expose the $11\bar{2}0$ plane, etching is performed parallel to the flat or the 0001 direction . However, it also will be understood that the sidewalls **100c** may not be orthogonal to the substrate **100**, but rather may be oblique thereto. Finally, it also will be understood that, although the sidewalls **100c** are shown in cross-section in Figure 1, the posts **100a** and trenches **100b** may define elongated regions that are straight, V-shaped or have other shapes. The spaced apart posts **100a** also may be referred to as "mesas", "pedestals" or "columns". The trenches **100b** also may be referred to as "wells".

Referring now to Figure 2, an optional conformal buffer layer **102** then may be formed on the substrate **100** including on the non-gallium nitride sidewalls **100c**, the non-gallium nitride tops **100d** and the non-gallium nitride floors **100e**. When the non-gallium nitride posts **100a** comprise silicon, the buffer layer may comprise silicon carbide and/or aluminum nitride. When the non-gallium nitride posts **100a** comprise silicon carbide, the buffer layer **102** may comprise high temperature aluminum nitride. Finally, when the non-gallium nitride posts **100a** comprise sapphire, the conformal buffer layer **102** may comprise low temperature gallium nitride and/or aluminum nitride. Other buffer layers may be used with these and other non-gallium nitride posts **100a**. The fabrication of a buffer layer on a substrate is well known to those having skill in the art and need not be described in detail herein.

Referring now to Figure 3, gallium nitride is grown on the non-gallium nitride posts **100a** including on the non-gallium nitride tops **100d**. More specifically, a gallium nitride layer **110** is formed, wherein the gallium nitride layer includes gallium nitride pyramids **110a** on the non-gallium nitride tops **100d**. These pyramids **110a** also may be referred to as "seed forms". It will be understood that the seed forms need not be pyramidal in shape but rather may have flash tops. As also shown in

Figure 3, second gallium nitride pyramids **110b** also may be formed simultaneously on the non-gallium nitride floors **100e**. Finally, a conformal region of gallium nitride **110c** also may be formed simultaneously on the sidewalls **100c** of the non-gallium nitride posts **100a**. Growth of the gallium nitride layer **110** preferably is performed using metalorganic vapor phase epitaxy (MOVPE) of triethylgallium (TEG), for example at 13-39 μmol/min and NH_3 at 1500 sccm in combination with 3000 sccm H_2 diluent, at low temperature, preferably at about 1000°C or less. Additional details of MOCVD growth of gallium nitride may be found in the above-cited publications to Nam et al, Zheleva et al., Zheleva et al. and Linthicum et al. Other growth techniques also may be used.

Details of the growth of gallium nitride layer **110** now will be described. In particular, as shown in Figure 3, the present invention preferably produces pyramidal gallium nitride seed forms **110a** on the tops **110d** of the gallium nitride posts **110a**. Earlier studies that were conducted on selective area growth of gallium nitride indicated that when gallium nitride pyramids are grown through mask windows, two regions of gallium nitride material result. One region is a relatively high defect density gallium nitride area that converges at the apex of the pyramid. The other region is nearly defect-free and encapsulates the pyramid. See, for example, the publication by Nam et al. entitled *Lateral Epitaxial Overgrowth of GaN Films on SiO_2 Areas via Metalorganic Vapor Phase Epitaxy*, Journal of Electronic Materials, Vol. 27, No. 4, 1998, pp. 233-237, the disclosure of which is hereby incorporated herein by reference.

According to the invention, the pyramids **110a** on the tops **100d** of the non-gallium nitride posts **100a** can form these same two regions. Once the nearly defect-free region is formed, the growth parameters can be changed to enhance lateral growth of gallium nitride from the relatively defect free regions of the pyramids, and that can result in nearly defect-free gallium nitride epilayers, as will be described below.

In particular, the pyramids preferably are formed at relatively low temperature, preferably about 1000°C or less using metalorganic vapor phase epitaxy, as was described above. The pyramids may be grown to have a width of about 2μm and a height of about 2μm on posts that are 1μm wide. In this case, the interior portions **110a'** of the pyramids **110a** having a width of about 1μm and a height of about 1μm, may have a high defect density of about 10^8 cm^{-2} or more, whereas the outer portions

110a" of the pyramids **110a** may be relatively low in defect, for example having defect density of about 10^5 cm^{-2} or less. The conformal layer **110c** on the sidewalls **100c** of the posts **100a** also may have a high defect density and the second pyramids **110b** on the floor **100e** also may have high defect density, for example greater than about 10^8 cm^{-2}. It also will be understood that in Figure 3, masks need not be used prior to or during the growth of the gallium nitride layer **110**.

Referring now to Figure 4, gallium nitride **120** then is preferentially laterally grown on the gallium nitride pyramids **110a**. Moreover, as shown in Figure 4, vertical growth also may occur. It will be understood that, as used herein, the term "lateral" means a direction that is orthogonal to the sidewalls **100c**. As used herein, the term "vertical" denotes a direction parallel to the sidewalls **100c**.

For stripes oriented along the $1\bar{1}00$ direction, the crystal morphology may change as the temperature increases. Thus, at lower temperatures, for example at about 1000°C or less, a pyramidal cross-section may result as was shown in Figure 3. At higher temperatures, for example at about 1100°C or more, a rectangular cross-section may result. Thus, by increasing the temperature, for example to about 1100°C or more, and preferably without changing any other growth parameters, gallium nitride **120** is preferentially laterally grown from the outer portions **110"** of the pyramids **110a**. Similar to ELO or pendeoepitaxy of gallium nitride, growth from the low defect outer portions **110a"** of the pyramids **110a** may have a lower density of line and planar defects. As shown in Figures 5 and 6, growth preferably is allowed to continue until the gallium nitride layer **120** coalesces on the tops **100d** of the posts **100a** to form a continuous gallium nitride semiconductor layer **130**. The trenches **100b** also preferably are filled with gallium nitride during this growth.

It will be understood that the III-V precursor ratio also may be changed during metalorganic vapor phase epitaxy to increase lateral growth relative to the vertical growth. It will be understood that the III-V precursor ratio also may be changed during seed form growth, to produce pointed or flat top seed forms. In particular, lateral growth may be enhanced by increasing the ammonia (Group V) flux and/or decreasing the gallium (Group III) flux, such that the overall V/III ratio increases. Once the gallium nitride layer **120** coalesces, vertical growth of the continuous gallium nitride layer **130** may be enhanced by decreasing the ammonia flux and/or by increasing the gallium flux, such that the overall V/III ratio decreases.

The growth of gallium nitride shown in Figures 3-6 need not use a mask Accordingly, a low defect continuous gallium nitride layer **130** may be fabricated without the need to form a mask on a gallium nitride layer. Process simplification thereby may occur. Moreover, the formation of the pyramids **110a** and the subsequent formation of the gallium nitride layer **120** may be performed in a single growth chamber, preferably by increasing the temperature and by leaving the other process parameters unchanged. Simplified processing therefore also may be provided.

Accordingly, low defect density gallium nitride semiconductor layers, having defect density of about 10^5 cm^{-2} or less may be grown on substrates including silicon, silicon carbide and/or other materials. Growth masks may be eliminated, and high quality gallium nitride may be formed in one growth run. The gallium nitride seed pyramids **110a** can confine the threading dislocations that stem from heteroepitaxial growth. Defect densities of less than about 10^5 cm^{-2} may be obtained within the volume of the laterally grown gallium nitride material. The maximum volume of the low defect density gallium nitride layer **130** need only be limited by the size of the substrate. Line defects that stem from the lattice misfit between the substrate and the epilayers preferably converge at the apex of the pyramid **110a'**, thereby confining most of the defects to the interior portion **110a'**.

Referring again to Figure 6, gallium nitride structures according to the present invention comprise a substrate **100** including a plurality of non-gallium nitride posts **100a** that define trenches **100b** therebetween. The non-gallium nitride posts **100a** include non-gallium nitride sidewalls **100c** and non-gallium nitride tops **100d**. The trenches include non-gallium nitride floors **100e**. A gallium nitride layer **100** is included on the non-gallium nitride posts **100a** including on the non-gallium nitride tops **100d**. The gallium nitride layer **110** preferably comprises gallium nitride pyramids **110a** on the non-gallium nitride tops **100d**. Gallium nitride regions **120** may be provided on the gallium nitride pyramids **110a**. Second gallium nitride pyramids **110b** also may be provided on the non-gallium nitride floors **100e**. A conformal gallium nitride layer **110c** also may be provided on the sidewalls **100c** between the gallium nitride pyramids **110a** and the second gallium nitride pyramids **110b**. The gallium nitride regions **120** preferably form a continuous gallium nitride layer **130**. The gallium nitride layer **110** also preferably fills the trenches. A conformal buffer layer **102** also may be provided on the substrate, wherein the

gallium nitride layer **110** is on the conformal buffer layer **102** opposite the substrate **100**.

In the drawings and specification, there have been disclosed typical preferred embodiments of the invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

What is Claimed is:

1. A method of fabricating gallium nitride semiconductor structures comprising the steps of:

providing a substrate including a plurality of non-gallium nitride posts that define trenches therebetween, the non-gallium nitride posts including non-gallium nitride sidewalls and non-gallium nitride tops, and the trenches including non-gallium nitride floors; and

growing gallium nitride on the non-gallium nitride posts, including on the non-gallium nitride tops.

2. A method according to Claim 1 wherein the growing step comprises the steps of:

growing gallium nitride pyramids on the non-gallium nitride tops; and

growing gallium nitride on the gallium nitride pyramids.

3. A method according to Claim 2 wherein the step of growing gallium nitride pyramids comprises the step of simultaneously growing gallium nitride pyramids on the non-gallium nitride tops and on the non-gallium nitride floors.

4. A method according to Claim 3 wherein the step of growing gallium nitride pyramids further comprises the step of simultaneously growing a conformal gallium nitride layer on the sidewalls, between the gallium nitride pyramids on the non-gallium nitride tops and on the non-gallium nitride floors.

5. A method according to Claim 2 wherein the step of growing gallium nitride on the gallium nitride pyramids comprises the step of growing gallium nitride on the gallium nitride pyramids until the grown gallium nitride coalesces to form a continuous gallium nitride layer.

6. A method according to Claim 5 wherein the step of growing gallium nitride on the gallium nitride pyramids further comprises the step of simultaneously filling the trenches with gallium nitride.

7. A method according to Claim 2 wherein the step of growing gallium nitride pyramids is performed at a first temperature and wherein the step of growing gallium nitride on the gallium nitride pyramids is performed at a second temperature that is higher than the first temperature.

8. A method according to Claim 7 wherein the step of growing gallium nitride pyramids and the step of growing gallium nitride on the gallium nitride pyramids are performed at same processing conditions other than temperature.

9. A method according to Claim 1 wherein the growing step comprises the steps of:

first growing the gallium nitride at a first temperature; and

then growing the gallium nitride at a second temperature that is higher than the first temperature.

10. A method according to Claim 1 wherein the following step is performed between the steps of providing and growing:

forming a conformal buffer layer on the substrate including on the non-gallium nitride sidewalls, the non-gallium nitride tops and the non-gallium nitride floors.

11. A method according to Claim 1 wherein the providing step comprises the steps of:

providing a non-gallium nitride substrate; and

etching the non-gallium nitride substrate to define the plurality of non-gallium nitride posts and the trenches therebetween.

12. A method according to Claim 9 wherein the first temperature is at most about 1000°C and wherein the second temperature is at least about 1100°C.

13. A method according to Claim 1 wherein the growing step comprises the step of masklessly growing gallium nitride on the non-gallium nitride posts, including on the non-gallium nitride tops.

14. A method according to Claim 1 wherein the non-gallium nitride sidewalls expose a $11\bar{2}0$ plane of the non-gallium nitride posts.

15. A method of fabricating gallium nitride semiconductor structures comprising the steps of:

providing a substrate including a plurality of non-gallium nitride posts that define trenches therebetween, the non-gallium nitride posts including non-gallium nitride sidewalls and non-gallium nitride tops, and the trenches including non-gallium nitride floors;

growing gallium nitride on the substrate at a first temperature; and then

continuing growing gallium nitride on the substrate at a second temperature that is higher than the first temperature.

16. A method according to Claim 15 wherein the first temperature is at most about 1000°C and wherein the second temperature is at least about 1100°C.

17. A method according to Claim 15 wherein the step of continuing growing comprises the step of continuing growing gallium nitride on the substrate at the second temperature until the gallium nitride forms a continuous gallium nitride layer on the substrate.

18. A method according to Claim 15 wherein the step of growing gallium nitride and the step of continuing growing gallium nitride are performed at same processing conditions other than temperature.

19. A method according to Claim 15 wherein the following step is performed between the steps of providing and growing:

forming a conformal buffer layer on the substrate including on the non-gallium nitride sidewalls, the non-gallium nitride tops and the non-gallium nitride floors.

20. A method according to Claim 15 wherein the providing step comprises the steps of:

providing a non-gallium nitride substrate; and

etching the non-gallium nitride substrate to define the plurality of non-gallium nitride posts and the trenches therebetween.

21. A method according to Claim 15 wherein the growing and continuing growing steps comprise the steps of masklessly growing gallium nitride and masklessly continuing growing gallium nitride.

22. A method according to Claim 1 wherein the non-gallium nitride sidewalls expose a $11\bar{2}0$ plane of the non-gallium nitride posts.

23. A method of fabricating semiconductor structures comprising the steps of:

providing a substrate comprising a first material, the substrate including a plurality of posts that comprise the first material and that define trenches therebetween, the posts including sidewalls and tops that comprise the first material, and the trenches including floors that comprise the first material; and

growing a second semiconductor material on the posts, including on the tops that comprise the first material.

24. A method according to Claim 23 wherein the growing step comprises the steps of:

growing pyramids of the second semiconductor material on the tops; and

growing the second semiconductor material on the pyramids.

25. A method according to Claim 24 wherein the step of growing the second semiconductor material on the pyramids comprises the step of growing the second semiconductor material on the pyramids until the grown second semiconductor material coalesces to form a continuous layer of the second semiconductor material.

26. A method according to Claim 23 wherein the following step is performed between the steps of providing and growing:

forming a conformal buffer layer on the substrate including on the sidewalls, the tops and the floors.

27. A method according to Claim 23 wherein the growing step comprises the step of masklessly growing the second semiconductor structure material on the posts, including on the tops that comprise the first material.

28. A method according to Claim 23 wherein the sidewalls expose a $11\bar{2}0$ plane of the first material.

29. A gallium nitride semiconductor structure comprising:

a substrate including a plurality of non-gallium nitride posts that define trenches therebetween, the non-gallium nitride posts including non-gallium nitride sidewalls and non-gallium nitride tops, and the trenches including non-gallium nitride floors; and

a gallium nitride layer on the non-gallium nitride posts including on the non-gallium nitride tops.

30. A structure according to Claim 29 wherein the gallium nitride layer comprises gallium nitride pyramids on the non-gallium nitride tops.

31. A structure according to Claim 30 wherein the gallium nitride layer further comprises gallium nitride regions on the gallium nitride pyramids.

32. A structure according to Claim 30 wherein the gallium nitride layer further comprises second gallium nitride pyramids on the non-gallium nitride floors.

33. A structure according to Claim 32 wherein the gallium nitride layer further comprises a conformal gallium nitride layer on the sidewalls, between the gallium nitride pyramids and the second gallium nitride pyramids.

34. A structure according to Claim 31 wherein the gallium nitride regions form a continuous gallium nitride layer.

35. A structure according to Claim 30 wherein the gallium nitride layer fills the trenches.

36. A structure according to Claim 29 further comprising:

a conformal buffer layer on the substrate including on the non-gallium nitride sidewalls, the non-gallium nitride tops and the non-gallium nitride floors, wherein the gallium nitride layer is on the conformal buffer layer opposite the substrate.

37. A structure according to Claim 29 wherein the structure is free of masking layers therein.

38. A structure according to Claim 29 wherein the non-gallium nitride sidewalls expose a $11\bar{2}0$ plane of the non-gallium nitride posts.

39. A semiconductor structure comprising:

a substrate comprising a first material, the substrate including a plurality of posts that comprise the first material and that define trenches therebetween, the posts including sidewalls and tops that comprise the first material, and the trenches including floors that comprise the first material; and

a layer of second semiconductor material on the posts including on the tops that comprise the first material.

40. A structure according to Claim 39 wherein the layer of second semiconductor material comprises pyramids of the second semiconductor material on the tops.

41. A structure according to Claim 40 wherein the layer of second semiconductor material further comprises regions of the second material on the pyramids.

42. A structure according to Claim 40 wherein the layer of second semiconductor material further comprises second pyramids of the second material on the floors.

43. A structure according to Claim 42 wherein the layer of second semiconductor material further comprises a conformal layer of the second semiconductor material on the sidewalls, between the pyramids and the second pyramids.

44. A structure according to Claim 41 wherein the regions of the second semiconductor material form a continuous layer of the second semiconductor material.

45. A structure according to Claim 39 wherein the layer of second semiconductor material fills the trenches.

46. A structure according to Claim 39 further comprising:

a conformal buffer layer on the substrate including on the sidewalls, the tops and the floors, wherein the layer of the second semiconductor material is on the conformal buffer layer opposite the substrate.

47. A structure according to Claim 39 wherein the structure is free of masking layers therein.

48. A structure according to Claim 39 wherein the sidewalls expose a $11\bar{2}0$ plane of the first material.

FIG. 1

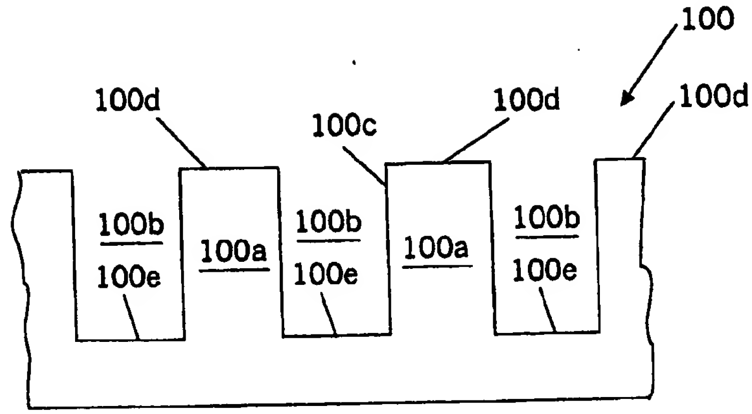


FIG. 2

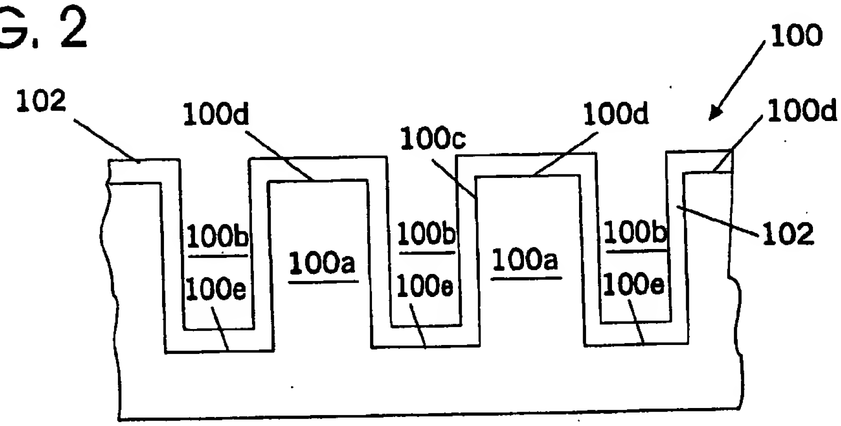


FIG. 3

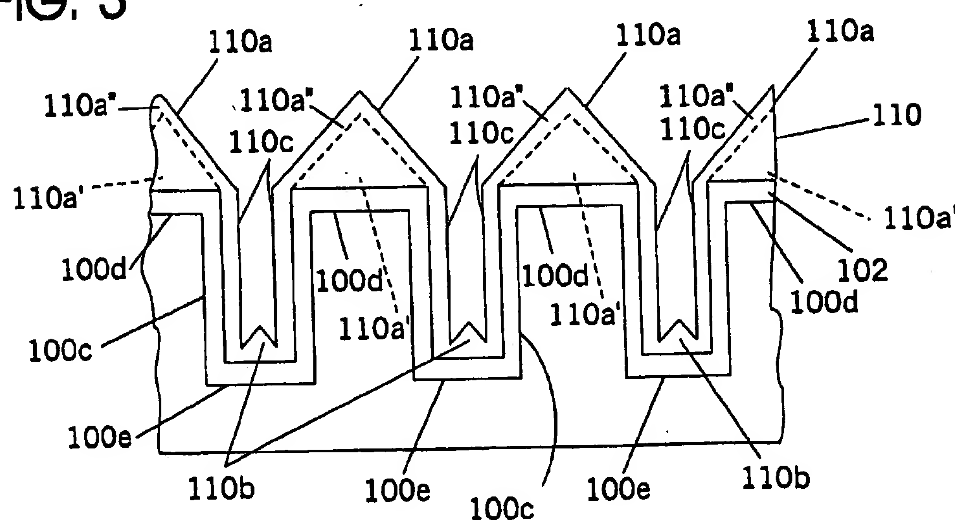


FIG. 4

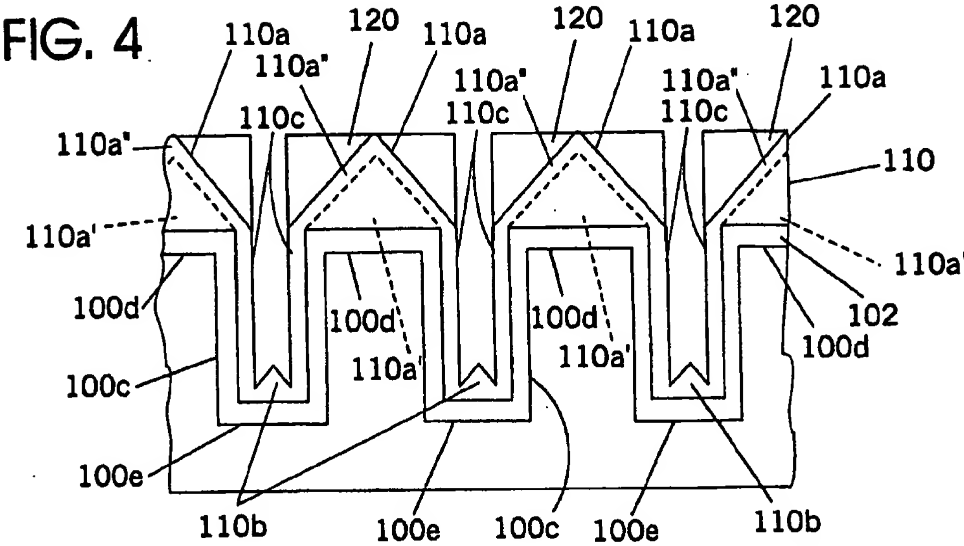


FIG. 5

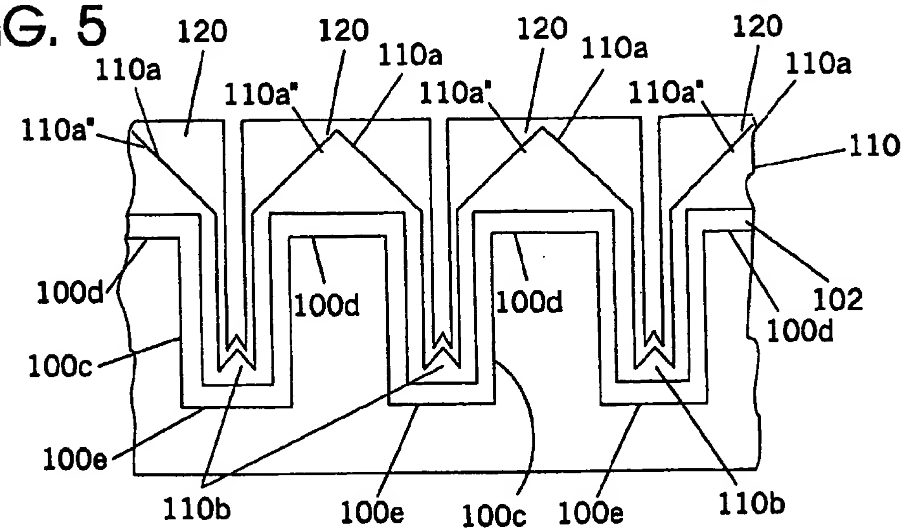
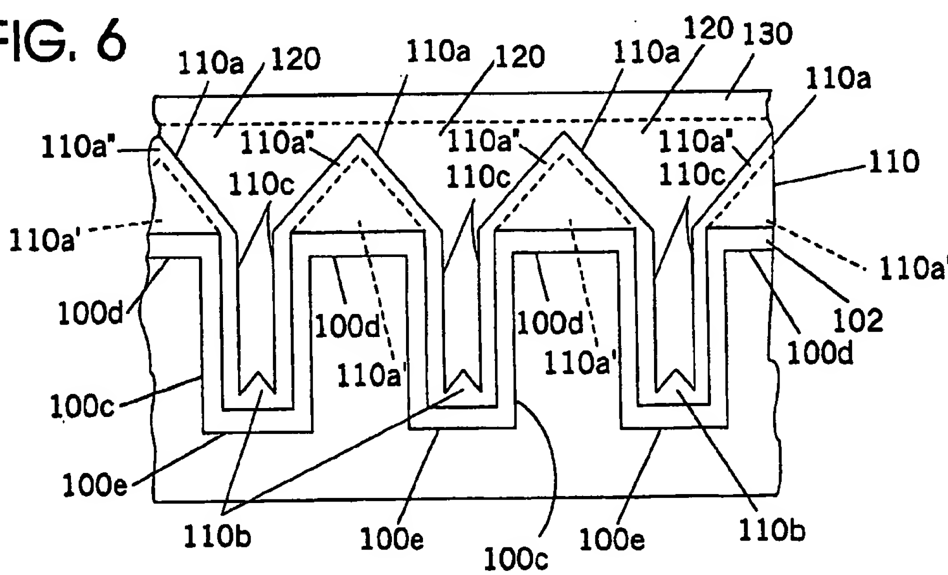


FIG. 6



INTERNATIONAL SEARCH REPORT

International Application No
PCT/US 00/40724

A. CLASSIFICATION OF SUBJECT MATTER
IPC 7 H01L21/20

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 7 H01L C30B

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

EPO-Internal, WPI Data, PAJ, INSPEC, IBM-TDB

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	WO 99 18617 A (CREE RESEARCH INC ;DOVERSPIKE KATHLEEN MARIE (US); LEONARD MICHELL) 15 April 1999 (1999-04-15) abstract; claims; figures page 9, line 14 -page 10, line 4 page 10, line 29 -page 11, line 29 ---	1,10,11, 13, 15-17, 19-21, 23,27, 29,37, 39,45,47

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[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
20 February 2001	27/02/2001

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

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A	ZENG K C ET AL: "OPTICAL PROPERTIES OF GAN PYRAMIDS" APPLIED PHYSICS LETTERS,US,AMERICAN INSTITUTE OF PHYSICS. NEW YORK, vol. 74, no. 9, 1 March 1999 (1999-03-01), pages 1227-1229, XP000805887 ISSN: 0003-6951 abstract; figure 1	1-3,15, 23,24, 29,30, 39,40
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